

20-25GHz Low Noise Amplifier

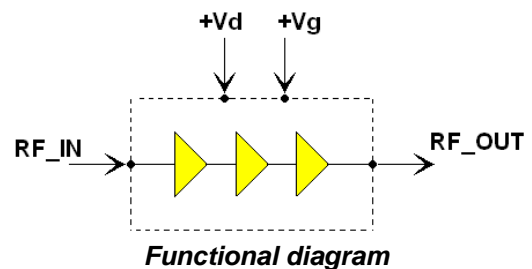
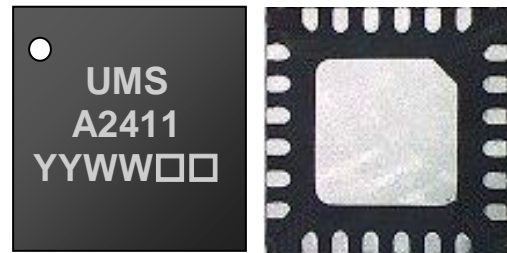
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA2411-QDG is a K-band low noise amplifier providing 26dB gain with a noise figure of 2.5dB from a single bias supply +5V.

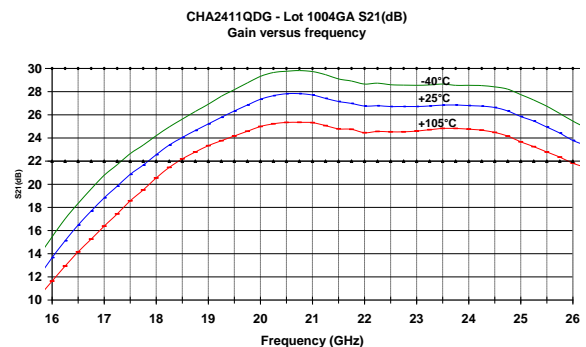
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 20-25GHz
- Excellent 2.5dB Noise figure
- 26dB ± 2dB stable Gain vs Temperature
- DC bias: Vd=5.0 Volt @ +I=43mA
- 24L-QFN4x4 SMD leadless package
- MSL1



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Frequency range	20		25	GHz
G	Linear Gain	22	26	30	dB
NF	Noise Figure		2.5		dB
RLoss	Input / Output Return Losses.		15		dB

Main Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Frequency range	20		25	GHz
G	Linear Gain	22	26	30	dB
$\Delta G(\text{Fop})$	Gain variation in frequency range		± 0.5		dB
$\Delta G(\text{T})$	Gain variation in temperature range		± 2		dB
NF	Noise figure		2.5		dB
RLoss	Input / Output Return RLosses.		-10		dB
$P_{-1\text{dB in}}$	Input Power at 1dB Gain Comp @24GHz		-14		dBm
IP3 in	Input IP3 @24GHz		-7.5		dBm
Pout_sat	Saturated Output Power @24GHz		13.5	15	dBm
+Vd, +Vg	Supply Voltage		5		V
+I	Supply Current		43	55	mA
Top	Operating temperature range	-40	25	105	°C

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

These performances have been obtained with the chip in QFN package mounted on the recommended boards (reference 95541) described in this document. These performances are highly dependent on this environment.

Absolute Maximum Ratings

Tamb.= +25°C⁽¹⁾

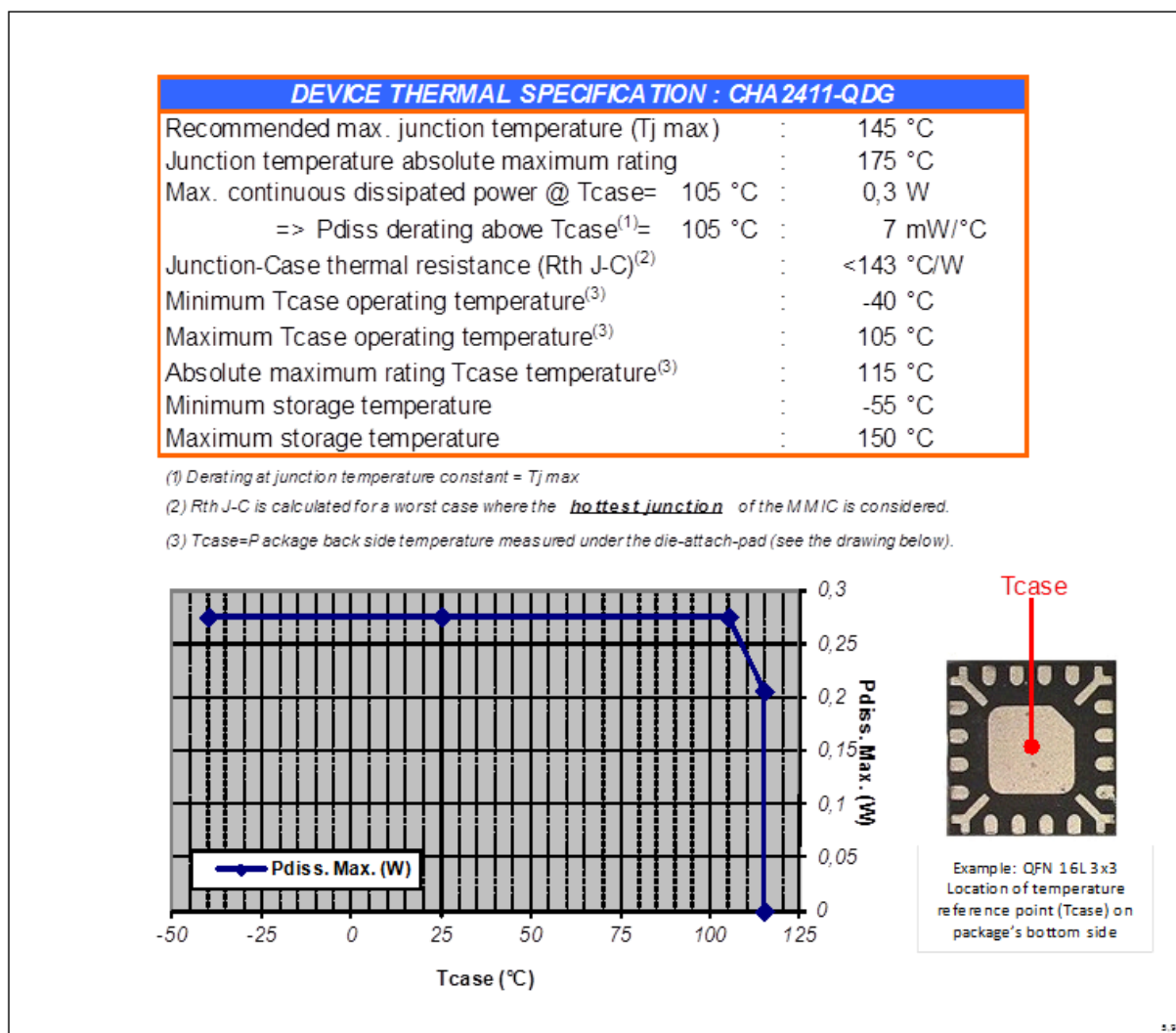
Symbol	Parameter	Values	Unit
+Vg, +Vd	Maximum positive supply voltage	6V	V
+I	Maximum positive supply current	65	mA
Pin	Maximum peak input power overdrive	-5	dBm
Top	Operating temperature range	-40 to +105	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage (duration < 1s)

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (T_{case}) as shown below. The system maximum temperature must be adjusted in order to guarantee that T_{case} remains below the maximum value specified in the next table. So, the PCB system must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the T_{case} temperature cannot be maintained below the maximum temperature specified (see the curve $P_{diss. Max.}$) in order to guarantee the nominal device life time (MTTF).

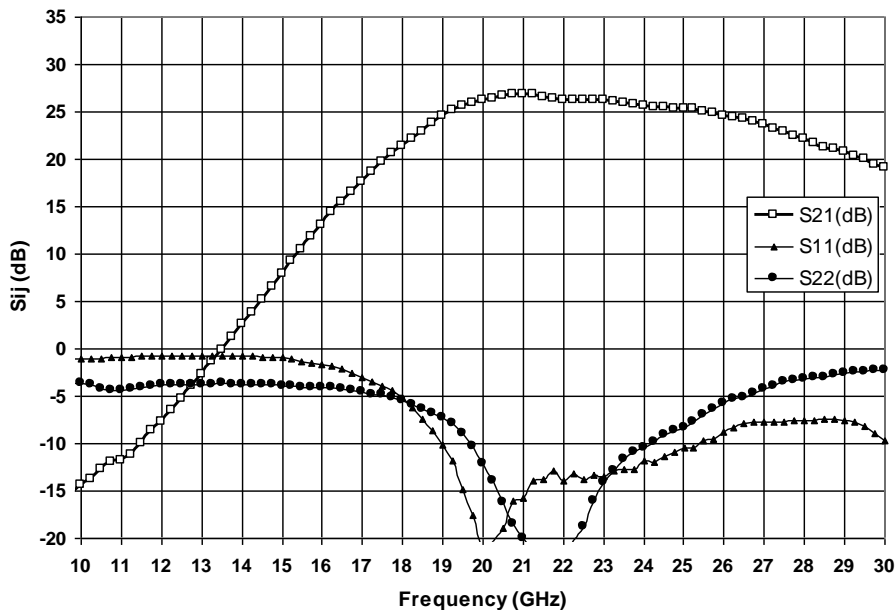


Typical Package Sij parameters

Tamb.= +25°C, Vd = +4.5V, Id = 43mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
10.0	-1.07	-49.55	-14.38	-58.07	-59.27	-175.76	-3.68	-21.83
11.0	-0.91	-68.36	-55.9	-102.44	-11.75	148.54	-4.36	-36.48
12.0	-0.78	-87.98	-54.01	-148.74	-7.68	126.87	-3.85	-53.87
13.0	-0.73	-107.81	-49.64	178.55	-2.72	98.18	-3.72	-73.42
14.0	-0.74	-128.9	-46.02	139.21	2.54	64.31	-3.71	-93.32
15.0	-0.98	-151.4	-46.54	107.66	7.85	24.67	-3.92	-113.67
16.0	-1.61	-176.03	-42.24	89.48	13.10	-21.61	-4.10	-133.26
17.0	-3.00	156.34	-42.85	34.58	17.64	-74.45	-4.56	-154.71
18.0	-5.18	123.53	-45.15	17.88	21.34	-132.27	-5.50	-179.79
19.0	-10.11	84.87	-50.38	-17.51	24.50	168.46	-7.22	152.98
20.0	-21.11	-6.32	-52.53	-49.82	26.22	104.07	-12.06	111.32
21.0	-15.70	-136.32	-55.01	127.63	26.76	42.30	-19.95	67.22
22.0	-13.98	-172.06	-47.39	77.30	26.20	-13.39	-21.91	-57.46
23.0	-13.50	-179.07	-64.30	-43.79	26.17	-64.30	-14.09	-87.97
24.0	-11.79	175.47	-41.92	19.85	25.62	-115.15	-10.50	-118.95
25.0	-10.43	165.19	-42.35	4.31	25.27	-163.45	-8.33	-136.39
26.0	-8.74	154.28	-41.19	-6.44	24.56	146.28	-5.78	-152.57
27.0	-7.78	131.33	-41.32	-17.81	23.64	96.46	-4.30	-170.04
28.0	-7.62	113.23	-39.65	-29.56	22.06	49.94	-3.15	170.66
29.0	-7.60	91.53	-38.35	-57.29	20.70	7.00	-2.55	155.07
30.0	-9.76	62.59	-39.18	-83.28	19.04	-39.18	-2.26	137.12

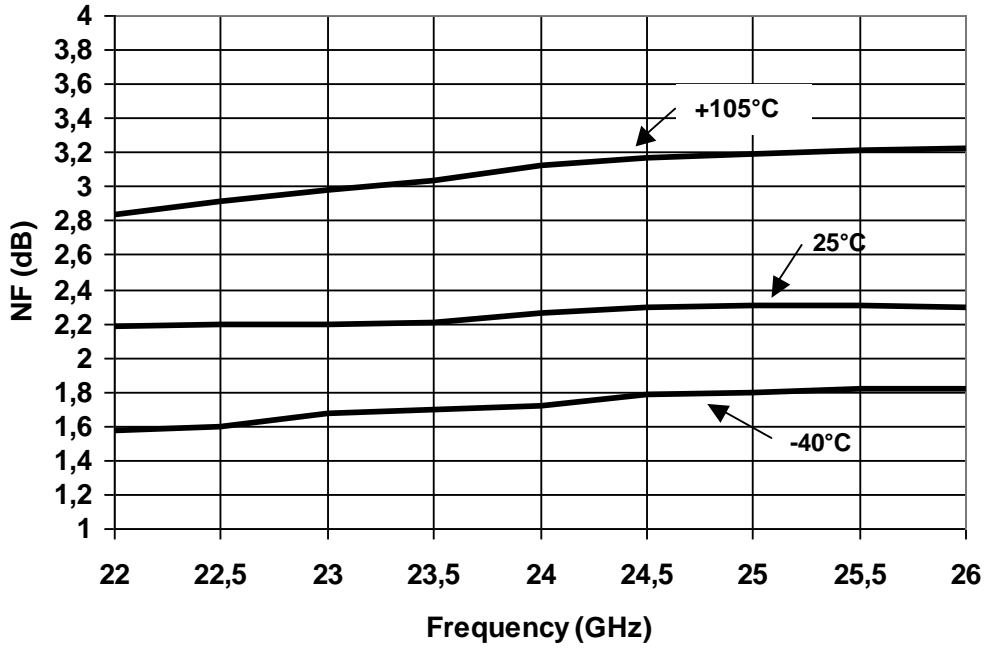
Typical Sij Parameters versus Frequency in the QFN package plans



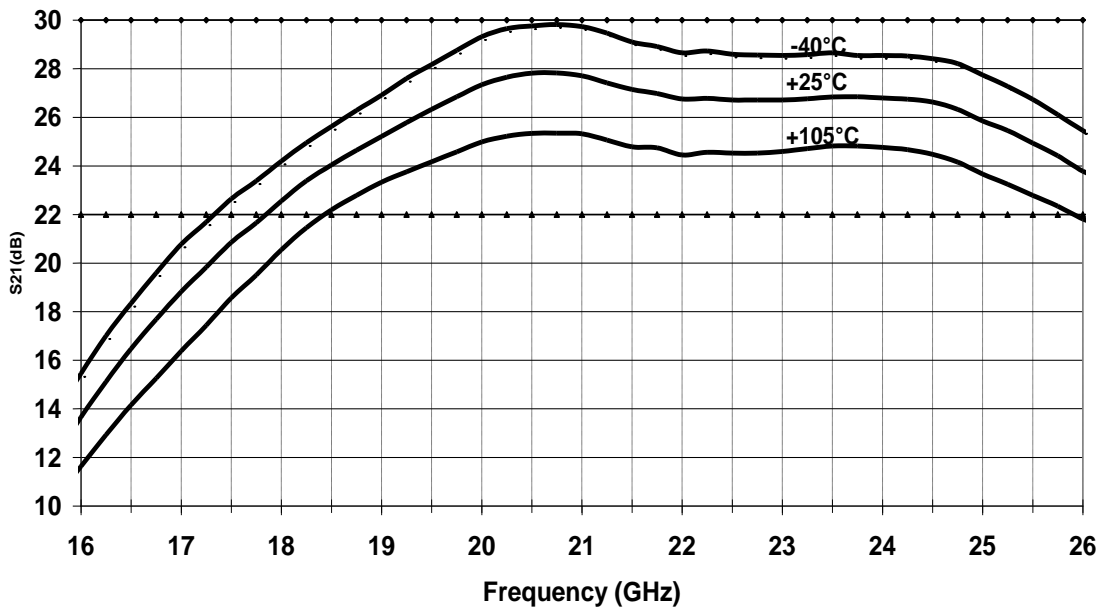
Typical Measurements on board 95541 (QFN plan)

Tamb.= -40°; +25°C; +105°C ,Vd = +4.5V / 55mA max

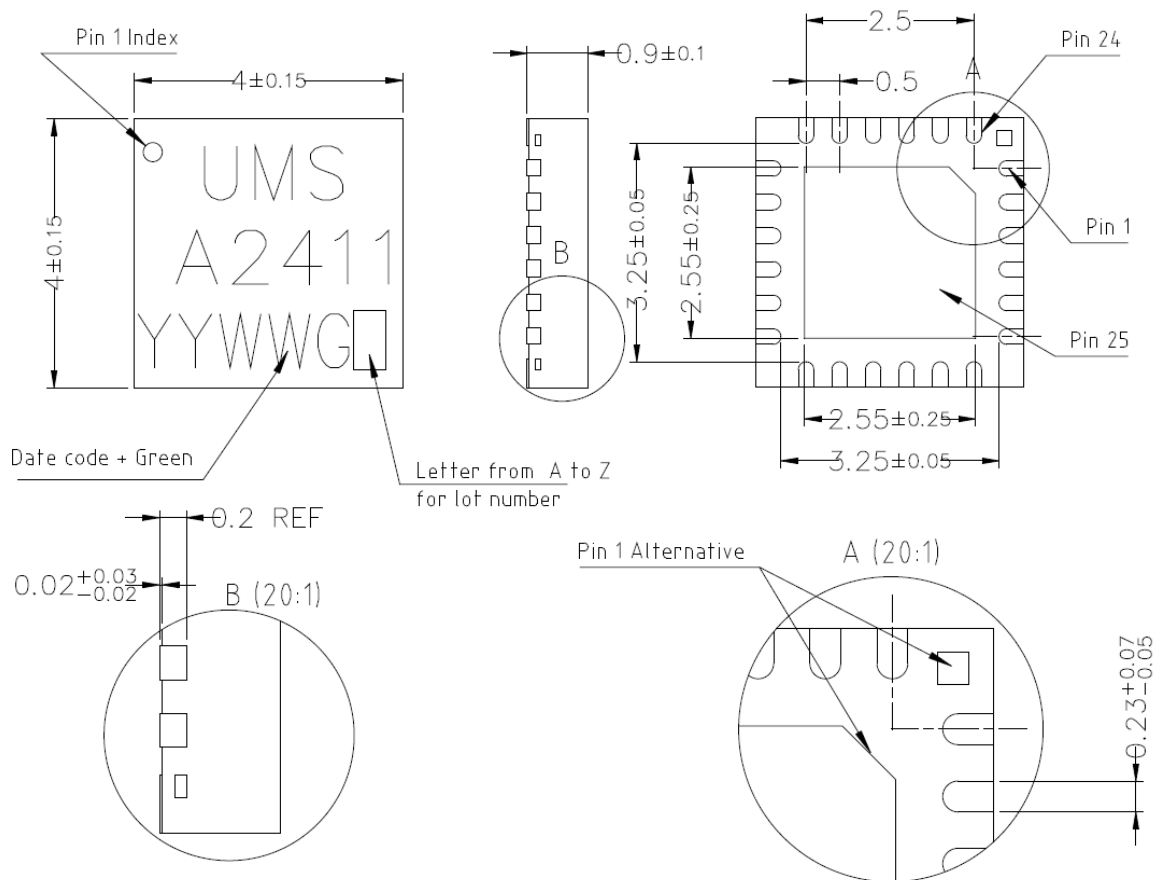
Noise Figure versus Frequency



Linear Gain versus Frequency



Package outline

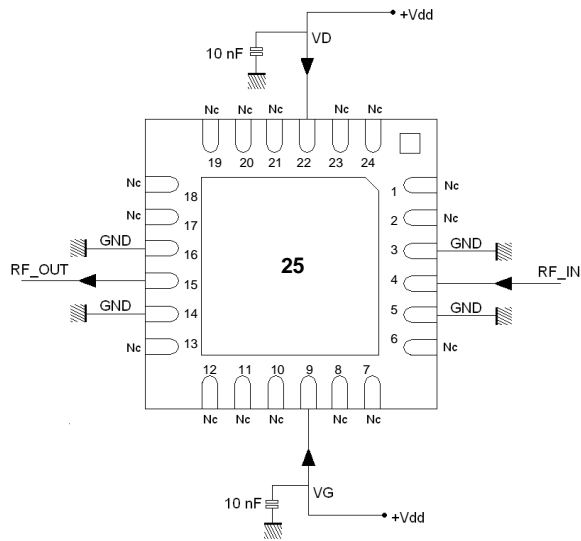


Matt tin, Lead Free	(Green)	1- Nc	13- Nc
Units :	mm	2- Nc	14- Gnd ⁽²⁾
From the standard :	JEDEC MO-220	3- Gnd ⁽²⁾	15- RF_OUT
	(VGGD)	4- RF_IN	16- Gnd ⁽²⁾
	25- GND	5- Gnd ⁽²⁾	17- Nc
		6- Nc	18- Nc
		7- Nc	19- Nc
		8- Nc	20- Nc
		9- VG	21- Nc
		10- Nc	22- VD
		11- Nc	23- Nc
		12- Nc	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

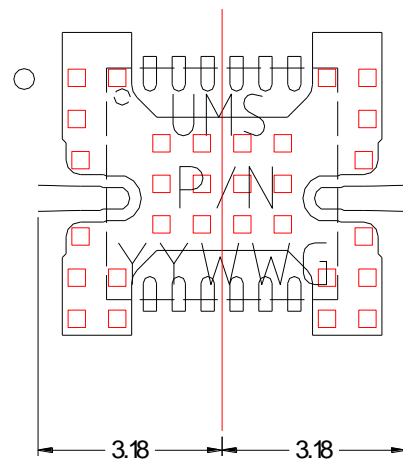
(2) It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

External Components and bias configuration (recommended)



Definition of the Sij reference planes

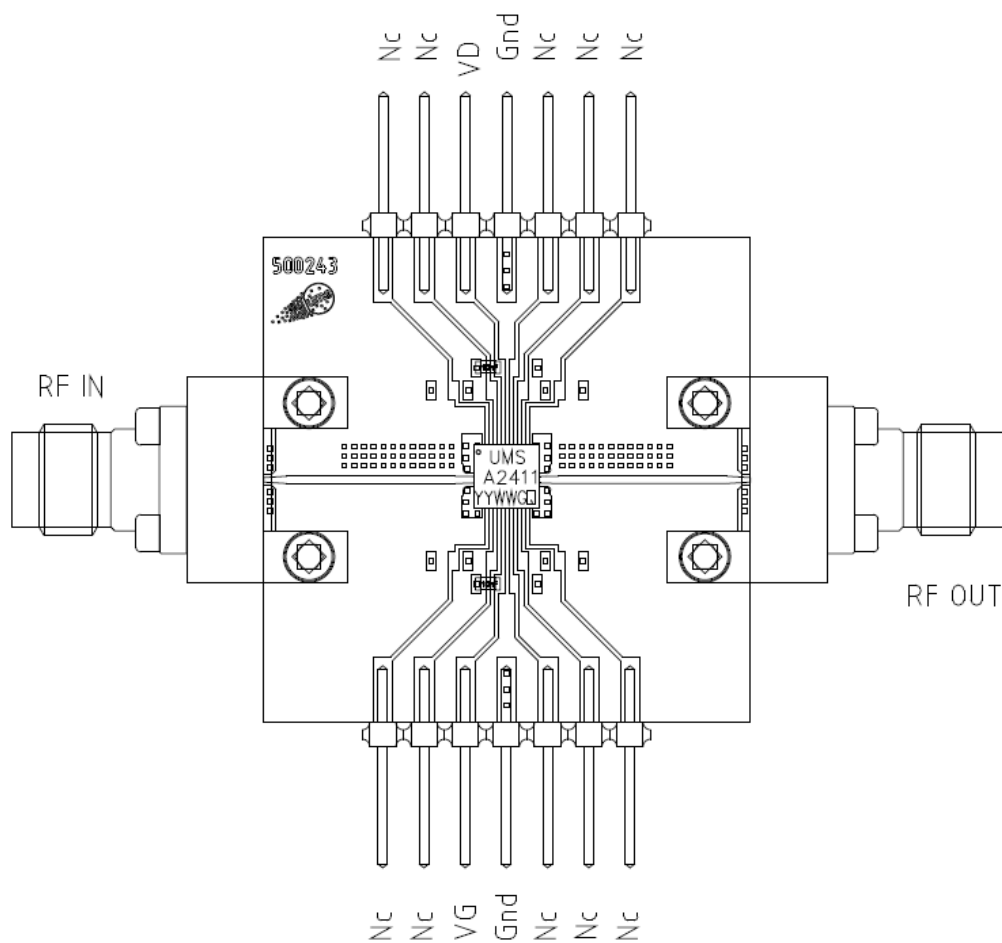
The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



Evaluation mother board

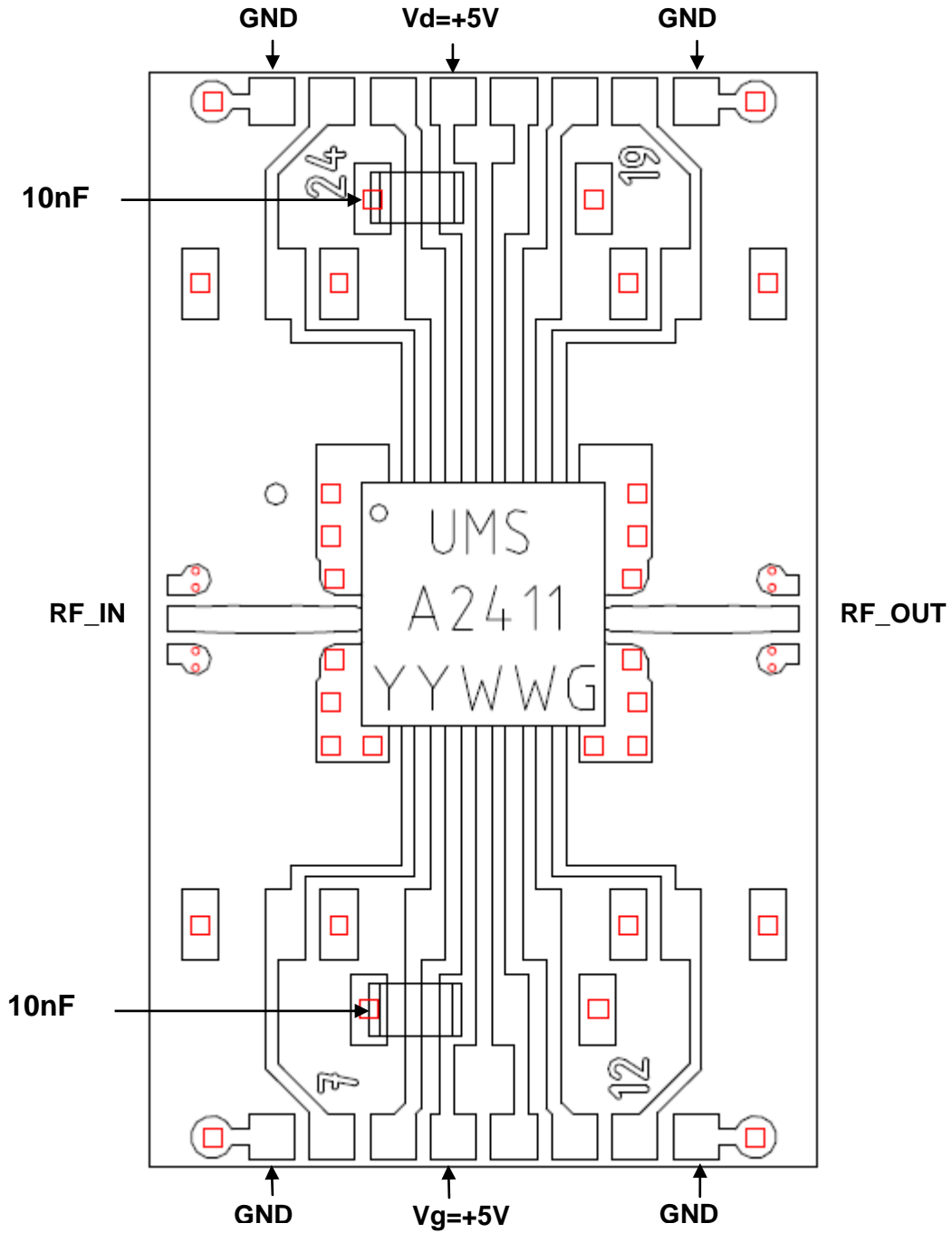
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF \pm 10% are recommended for all DC accesses.
- See application note AN0017 for details.

Recommended Test fixture (Ref. 500243) for measurements over temperature range



Evaluation mother board

Recommended Test fixture (Ref. 95541) for measurements over temperature range (unit=mm)



Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN4x4 RoHS compliant package:

CHA2411-QDG/XY

Stick: XY = 20

Tape & reel: XY = 21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**